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A Review on Performance Evaluation of Multilevel Multifunctional GridConnected Inverter Topologies and Control Strategies Used in PV Systems

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Abstract: Day by day, the popularity of multi-level inverters (MLIs) for applications of high power and high voltage is growing. These MLIs, including solar photovoltaic (PV) systems, are being built into the grid for renewable energy extraction. The MLI induces a low harmonic material staircase output voltage and can pump a sinusoidal grid current with an increased power factor. The MLI based grid tied PV system will therefore work with reduced filter requirements at the lower switching frequency. The numerous MLIs, modulation and control techniques for grid connected applications are discussed in this article. A detailed classification of different grid connected multi-level inverters (GCMLIs) based on the number and arrangement of DC voltage sources is presented. For various MLI based PV systems that communicate with the utility grid, various control techniques and modulation techniques have also been addressed. For a deeper understanding and reliability of past and future PV system technologies, this paper also provides detailed comparisons and discussion of different control techniques used in single phase and three phase grid connectedMLI.

Keywords: Multi-level inverter (MLI), Solar Photovoltaic (PV), Control techniques, Modulation strategies,Grid connected multi-level inverters (GCMLIs)

INTRODUCTION

Photovoltaic (PV) electricity installations have seen considerable development in recent years, when the worldwide installed solar power capacity grew from 1.2 GW in 1992 to 227 GW in 2016 (World Energy Council, 2017). About 1% of the total energy used worldwide is generated by solar systems (Renewable Energy Statistical Review, 2017). Among the PV systems that are standalone (Daher et al., 2008) and attached to the grid (Elrayyah et al., 2015; 19-29), the latter accounts for over 99% of the overall PV installations (Elrayyah et al.,

al., 2015; Kouro et al., 2015). This is due to reduced construction costs, scalability, lower downtime and better stability of grid-connected networks over standalone systems in their potential growth (Elrayyah et al., 2015; Kouro et al., 2015). Conventional two-level inverters were found to be unsuitable for the medium and high- voltage power grid when used as an interface between PV sources and the grid (Myrzik, 2001; Kjaer et al., 2005)due to a lower number of output voltage levels (Colak et al., 2011a) and thus, greater harmonics in the injected grid current. For interfacing with the medium and high voltage utility grid, multilevel inverters (MLIs) (Colak et al., 2011a), which came into being in 1975, are rather suitable. With reduced harmonics and THD, reduced dv/dt tension on switches, less need for passive filters, lower torque ripple when used for motor drives, and can provide fault-tolerant operation, the MLIs have always provided a higher quality output voltage waveform (Abu et al., 2010; Gupta and Jain, 2010; Franquelo et al., 2008). A significant number of switching devices and associated gate driver circuitry require the disadvantages associated with the most common typical MLIs such as cascaded converter, neutral point clamped (NPC) and flying capacitor (FC). In contrast with two-level inverters, this raises the complexity of the entire MLI circuit and decreases efficiency (Nabae et al., 1981; Ayoub and Saad, 2007; Jana et al., 2016, 2017; Pavan and Atul, 2015; Lezana and Aceiton, 2011; Babaei and Gowgani, 2014; González et al., 2008; Sowjanya and Veerendranath, 2014). These drawbacks have driven researchers to focus on various modular inverter architectures (Bailu et al., 2015; Mei et al., 2013; Grandi et al., 2009); asymmetric (Babaei et al., 2013; Chattopadhyay and Chakraborty, 2017; Fengjiang et al., 2015), Wu et al., 2017), and hybrid (Franquelo et al., 2008; Nabae et al. These MLIs can be directly connected with a high-voltagephotovoltaic (PV) system and utility grid, meaning the transformer has less operation (Sandeep et al., 2018).

Modulation strategies for the MLI also play a very important role in improving the efficiency and harmonic content of the output voltage and grid current profile (Zhao et al., 2010b). Based on the switching frequency used, the pulse width modulation (PWM) techniques can be narrowly classified under three distinct categories ashigh switching frequencies that can be applied to the MLI based on the design and implementations. The techniques of high frequency sinusoidal pulse width modulation (SPWM) are comparatively easy to apply (Carrara et al., 1992; Naderi and Rahmati, 2008; Mcgrath and Holmes, 2002; Zhao et al., 2010a; Alexander, 2016; Kumar and Narayanan, 2016; Vadhiraj et al., 2013; Sahoo and Bhattacharya, 2018; Roberto et al., 2011) and are therefore very common for multilevel connected single and three-phase Grid For three phase MLI setups, such as three phase AC drives and three phase grid linked applications for better DC connection voltage utilization and reduced common mode voltages, the SVPWM technique is more widespread.

As most of the MLI needs multiple DC sources, there is also a certain amount of DC-linked tensile balance problems with certain typical problems of a PV system when interfacing PV

systems connected to the grid, suchas injecting solely sinusoidal grid current into the unit power factor (Jana et al., 2016; Madan et al). The utilitieshave also developed several special norms and specifications (grid codes) for connecting PV systems to grid to preserve the high power quality, DC current injection, flicker, frequency, injected current harmonics, total harmonic distortion, (THD) and photovoltaic power factor (Elrayyah et al., 2015). The problems with harmonics can be overcome by using MLI and PWM techniques and obtaining pure sinusoidal grid current at relatively lower frequencies with minimal passive filter components than the traditional two-stage inverters (Young et al., 1999; Hung et al., 1993; Silva, 1997). However, effective grid synchronization and control are required to protect the above grid codes (Silva, 1999; Kumar et al., 2016; Nasrudin and Selvaraj, 2010; Sun et al., 2013; Ellabban and Abu-Rub, 2016; Yang et al., 2013; Wu and Li, 2015; Xiaojie et al., 2017a, 2017b; Xu et al., 2007; Mostafa et al., 2013; Manoharan et al., 2017; Kouro et al., 2007, 2009; Model, 2011; Rodriguez et al., 2013, 2014; Guzinski and Abu-Rub, 2013; Trabelsi et al., 2013; Rivera et al., 2012; Sanchez et al., 2012; Kazmierkowski et al., 2011; Cortes et al., 2008). An analysis of the topology of MID voltage sources, considering conventional three-phase inverters, was carried out by Meneses et al. (2013) and Zeng et al. (2013). Often, only three different kinds of closed loop management methods have been discussed. Some grids linked to MLI (GCMLI) and their control was checked by researchers from Colak et al. (2011b) and Barghi et al. (2015). However, GCMLIs and modulation techniques were not detailed in the paper and the control topologies were mostly traditional. A study of the essence of the MLI switches and their modulation techniques was carried out in Natarajan and Kaliannan (2017). The paper does not consider any MLIs and their control strategies aligned with the grid (GCMLI). The breakthrough in this article is the thorough analysis of recent work on the various classic and reduced multilevel inverters (MLI) in the implementation of grid connections. Also presented are the classifications and modulation of multilevel grid connected inverters for PV. In addition, the most up-to-date monitoring methods to resolve the issues associated with grid PV systems are closelyreviewed.

Grid Connected PV Inverters

The inverters connected to the grid can be categorized on the basis of power rating and the PV module configuration (Kouro et al., 2015). Smaller (within a few watts to several kW), medium (within a few kW to several hundred kW), and big (a few hundred to several hundred kW) PV systems are generally PV systems depending on the power level. PV systems are categorized as smaller. The PV modules can be arranged generally in four different configurations based on the different types of inverters (Kouro et al., 2015) which are discussed as follows:

Module Integrated Inverter

These small inverters are also called micro-inverters, with a lower power rating (Kouro et al., 2015). The PV modules (back of each PV module) are separately connected by the MPPT

controller (Maximum Power Point Tracking). In the figure is shown the schematic diagram of such a PV system. The PV system, an additional DC- DC conversion stage and a high-frequency transformer for galvanic isolation or line frequency up transformer are mandatory because of the low power supplied by Module Inverters (Elrayyah et al., 2015; Kouro et al., 2015). These configurations reduce the total performance of the conversion unit. The use of high MPPT accuracy, due to the fastest energy transfer from the PV system, compensates this downside. The integrated module inverters use MOSFET and typically are favored for low cost and small scale PVsystems.

(a)Module Inverter (b) String Inverter (c) multistring Inverter (d)

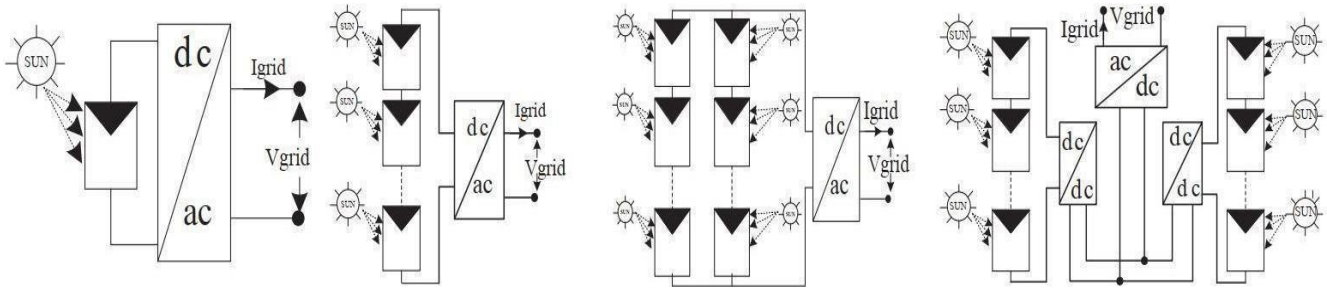


Figure 1: Classification of conventional inverters interfaced with grid connected PV system, based on thePV-module arrangement (Kouro et al., 2015).

String Inverter

As seen in Fig, in the string inverter. 1(b) there is no additional DC-DC conversion and galvanic insulation to make the device more effective (Kouro et al., 2015). String inverters however have less exact MPPT and less energy input than the built-in inverters module. The PV systems, particularly for residential use, are often used for medium size inverters.

Multistring Inverter

The goal of the multiple inverter creation is to flexiblize the current string inverter (Elrayyah et al., 2015; Kouro et al., 2015). Figure displays the schematic diagram of a multi transmission inverter PV system. The string is attached here to increase the voltage of the tinier strings through separate MPPT and DC-DC conversion levels. These inverters are usually favorite for residential or commercial uses in medium and large scale PV plants.

Central Inverter

The entire PV array is interfaced with the grid through a center inverter consisting of several parallel strings as seen in the fig.1 (d). The big downside of the central inverter is the use of MPPT, resulting in poor power yields from a photovoltaic system and unable to solve power problems that vary (Kouro et al., 2015). However, the inverter is applicable to large scale PV systems with a single conversion stage and IGBT use (Elrayyah et al., 2015; Kouro et al., 2015). Central inverter performance improved from 92 percent in the 1990ies to 98.8 percent in 2010, delivering good stability and full working life (Elrayyah et al. 2015). However, only two voltage levels are created by the above grid-connected inverters. The inverter must therefore be run on a high frequency (more than 20 kHz) and a hard filter

circuit for the grid current sinusoidal operation. In addition to this, the higher switching stresses, have more switching losses, more EMI problems and have limited energy carrying capability.

Grid Connected Multilevel Inverter (GCMLI) Topologies

Recently, the multi-level GCMLIs are used in combination with renewable energy sources, and have become popular (Jana et al., 2016). The GCMLI topologies are commonly classified as conventional MLIs, with lower switch MLIs. However, this section offers a thorough grading of PV-fed GCMLIs based on the number of DC sources (PV sources) and arrangements needed to supply the inverters (see Fig. 2).

Neutral Point Clamped MLI (NPCMLI)

The neutral point clamped MLI (NPCMLI), also known as a diode clamped MLI (DCMLI) (Franquelo et al.,2008), was first introduced by Baker and Bannister in the year 1980. For a generalized m-level NPC inverter, the per phase inverter circuit comprises 2(m − 2) clamping diodes, (m − 1) number of DC link capacitors and 2(m − 1) number of switches. Fig. 3(a) shows a grid connected five level NPCMLI with eight switches (S1, S2, …, S8)and four DC bus capacitors (C1, C2, C3 and C4). The positive voltage levels (+Vdc/4, +Vdc/2) are obtained byturning on the switches S1, S2, S3 and S4; while the negative voltage levels (−Vdc/4, −Vdc/2) are obtainedby turning on the switches S5, S6, S7 and S8. The zero voltage level is obtained by turning on the switchesS3, S4, S5 and S6. Such MLIs are very useful, especially for three phase applications as they use only single DC source for any number of voltage levels. However, the major drawbacks of the NPCMLI are lack of modularity, difficult to balance the DC link voltage equally amongst the DC link capacitors for more than three outputvoltage levels, restricting it for higher voltage (Abu et al., 2010; Gupta and Jain, 2010) and ac motor driveapplications (Franquelo et al., 2008).

Flying Capacitor MLI (FCMLI)

The flying capacitor MLI (FCMLI), also known as clamping capacitor MLI (CCMLI), was first introduced by

Menard and Foch in the year 1992 (Nabae et al., 1981). Similar to NPCMLI, the m-level FCMLI also requires(m − 1) DC bus capacitors, 2(m − 2) clamping capacitors and 2(m − 1) number of switches. Fig. 3(b) depicts a grid connected five- level FCMLI, comprising eight IGBT switches (S1, S2, … , S8) and four DC bus capacitors (C1, C2, … , C4). The positive phase voltage levels (+Vdc/4, +Vdc/2) are attained by turning on the switches S1, S2, S3 and S4; while the negative voltage levels (−Vdc/4, −Vdc/2) are ob- tained by turning on the switches S5, S6, S7 and S8. The zero-voltage level is obtained by turning on the switches S1, S2, S5 and S6 or S3, S4, S7 and S8. The FCMLI offers many advantages over NPCMLI in terms of, modularity, easily extendable structure and capacitor voltage balancing even for the higher voltage levels. However, the major problem with FCMLI is its expensiveness (due to

the large number of capacitors) and complex control circuitry

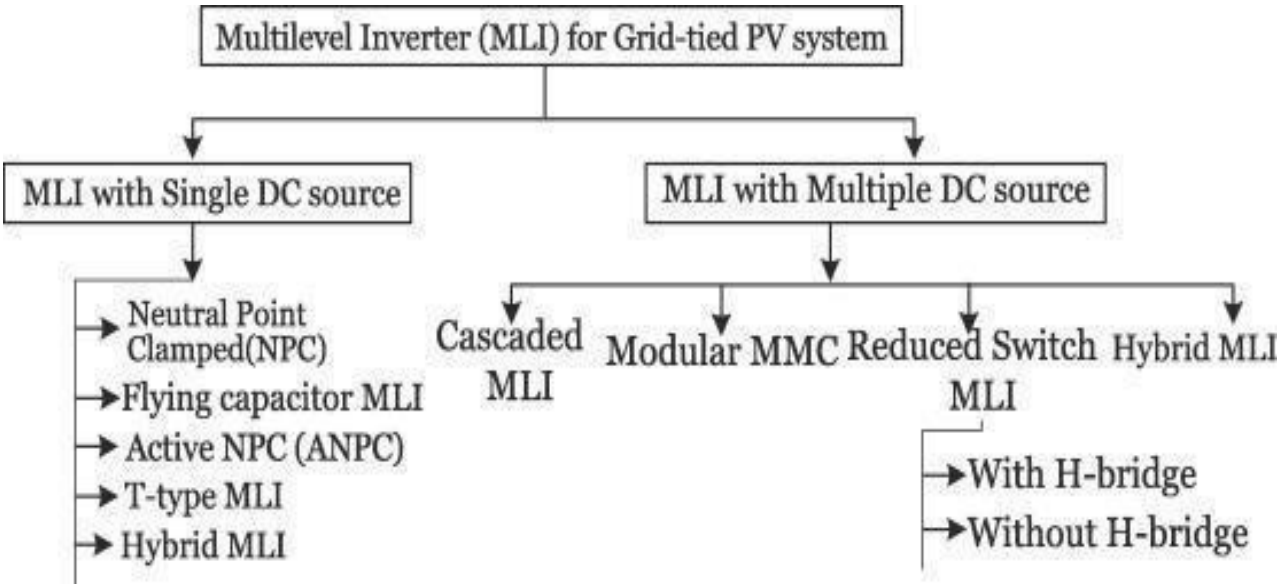


Figure 2: Classification of multi-level inverter based grid connected PVsystems.

Active Neutral Point Clamped (ANPC) GCMLI

ABB initially suggested the topology for active neutral clamped point (ANPC) (Ayoub and Saad, 2007). The ANPC MLI improves compared with NPC MLI since two additional voltage stages (five levels) were generated by connecting a phase condenser to a tri-level NPC converter. The topology consists of four IGBT's (S1, S1', S2,S2') and four MOSFET's (S3, S3', S4, S4'), which serve as external switches, operating at a far lower frequency. The circuit in the fig.3(c), will achieve an output tension of five levels if DC communication condensers are balanced (C1, C2 and one fourth of the DC voltage used is used over the additional step condenser (C). By producing high-quality output voltage, the converter uses a reduced number of low voltage switches. The topology is commonly used for applications of industrial drive (Nabae et al., 1981).

T-Type MLI

In order to reach a higher voltage level in the reduced number of instruments, the T- type MLI was introduced in Jana et al. (2016). The 7 stage MLI in the Fig. 3(d) contained one H-bridge and two bidirectional switches (H1, H2, H3 and H4) (S1, S2). The number of bidirectional switches along with condensers at the CD connector must be increased to further raise the voltage levels.

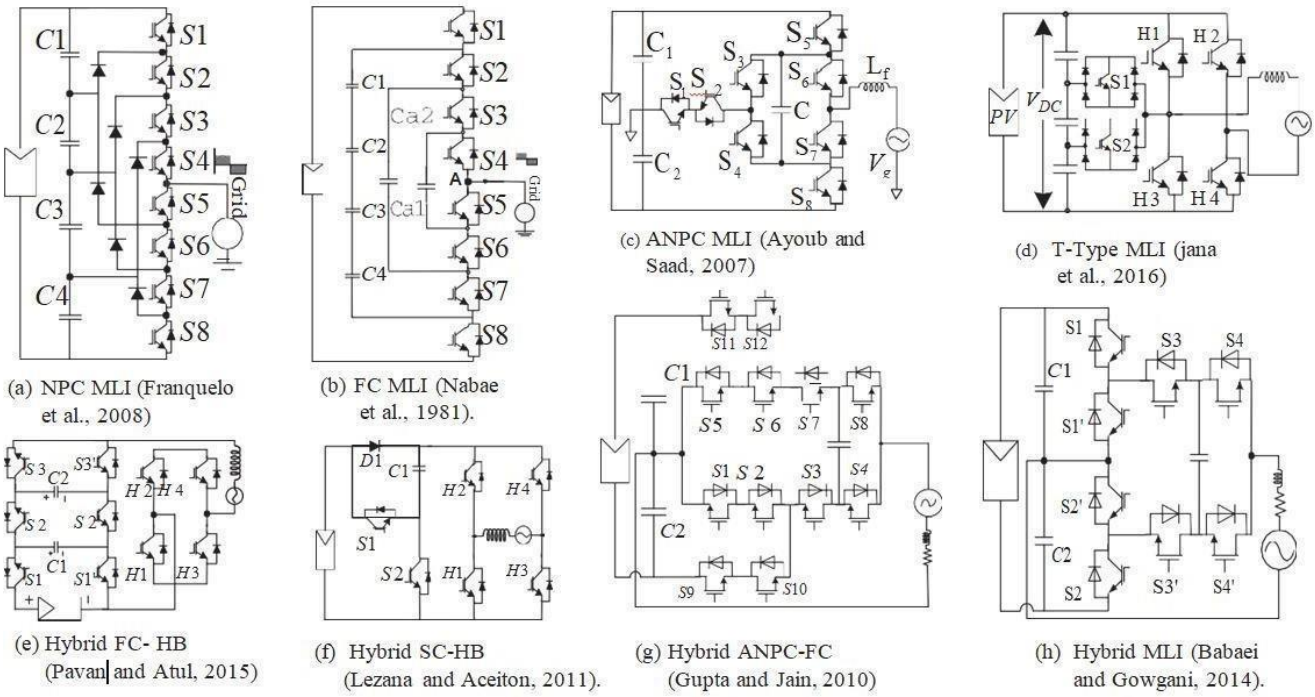


Figure 3: Power circuit of GCMLIs with single DC (PV) source.

Hybrid MLI Topology with Single Voltage Source

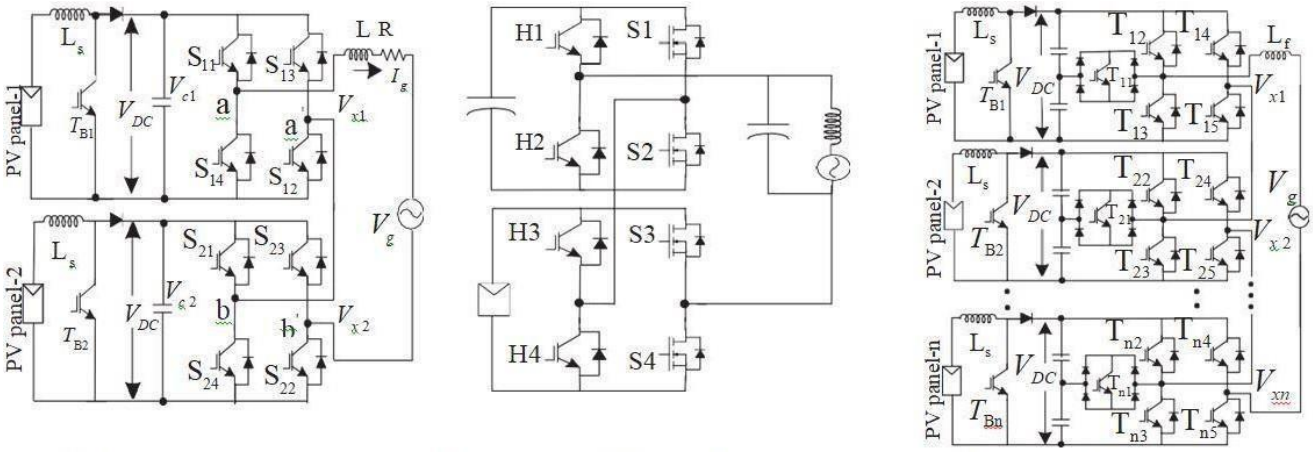
A hybrid MLI is one of the newest developments for higher voltage levels with the combination of two or more topologies. A three-cell 7-grade flying capacitor (FCMLI) with one H-bridge (HB) in Pavan and Atul (2015) is combined to achieve 15 voltage levels, as shown in Fig.3(e). This hybrid topology's switches are complementary. fig.3(f) reflects a more hybrid topology that incorporates a three-story hybrid conversion converter (SC) with one HB for five voltage levels (Lezana and Aceiton, 2011). This MLI configuration refers to both symmetric sources and asymmetric sources of voltage. The Hybrid ANPC-FC (Gupta and Jain, 2010) converter blends the properties of MLI Flying condenser (FCMLI) with NPCMLI (neutral spacer) inverter. fig 3(g). In comparison to NPC, the architecture of this hybrid topology with the potential to voltage balance except for a higher voltage level is very scalable. Fig. 3(h) shows a similar hybrid MLI with reduced switch as proposed in Babaei and Gowgani (2014).

Cascaded Grid Connected MLI (GCMLI)

The cascaded MLI H-Bridge (CHBMLI) topology is primarily a sequence connector of a variety of single-stage inverters to isolated dc sources (Soviania and Veerendranath 2014). It consists of 2 (m −1) power switches and (m − 1)/2 DC voltage sources to achieve m of voltage output speeds. Fig.4(a) represents a eight IGBT and two PV sources five stages CHB inverter. The three voltage levels of +VDC, 0 and −VDC can be produced at each H- bridge. Combining the voltages produced by Two H-Bridges, the desired output voltage can thus be achieved with almost all renewable energies. In comparison to other typical MLIs (NPC

and FC), the CHB topology is compact and modular, since there are no clamping diodes or cumbersome condensers and their balancing problems. The PV services are supplied by the dc-dc converter to the CHB inverter as seen in the Fig.4(a).The cascaded MLIs are further classified as symmetric and asymmetric ones, on the basis of equality of DC voltage sources (Jana et al., 2017). When the value of all the DC voltage sources is equal, the CHB is said to be Unary or

symmetrical. The asymmetric CHBMLI (unequal DC sources) can further be classified as binary (voltages in the ratio of 2) and trinary (voltages in the ratio of 3) configurations. The binary asymmetric CHB inverter where, the DC link voltages are chosen in the ratio 20Vdc: 21Vdc: ⋯ :2n−1Vdc (Mahato et al., 2017) as compared to 30Vdc: 31Vdc: ⋯ :3n−1Vdc in the trinary configuration (Babaei et al., 2013). To generate a voltage of m- level, the binary CHBMLI requires (m + 9)/8 number of H-bridge cells compared to (m/9 + 3)/2 cells in the trinary configuration. However, in the conventional symmetrical CHBMLI, the (m − 1)/2H-bridge cells are required to generate the same output voltage levels. Cascaded H-bridge (CHB) with a flying capacitor (Chattopadhyay and Chakraborty, 2017), contains two H-bridge inverters with one of the bridges being fed by a flying capacitor (FC) as shown in Fig. 4(b). The DC sources are arranged in the trinary fashion (30:31) in order to generate the nine level output voltage. Thus, the voltage across the FC is always maintained one third of the DC link voltage of the other bridge under steady state conditions. The capacitor voltage is balanced by a complex capacitor balancing technique that operates the MOSFET switches in one leg of the inverter at high switching frequency. A single phase grid connected cascaded MLI is reported in Jana et al. (2016) using T-Type inverter. The basic T-type module consists of five switches that can generate a voltage of five levels. For high level grid application, several identical T-type inverter modules can be cascaded as shown in Fig. 4(c) to achieve the desired grid voltage. For an m-level inverter, (m − 1)/4 basic symmetrical modules are required, which is just half of the conventional cascaded H- bridge inverter.



(a) CHB (Sowjanya and Veerendranath, 2014)

(b) Asymmetrical CHB with FC (Chattopadhyay and Chakraborty, 2017)

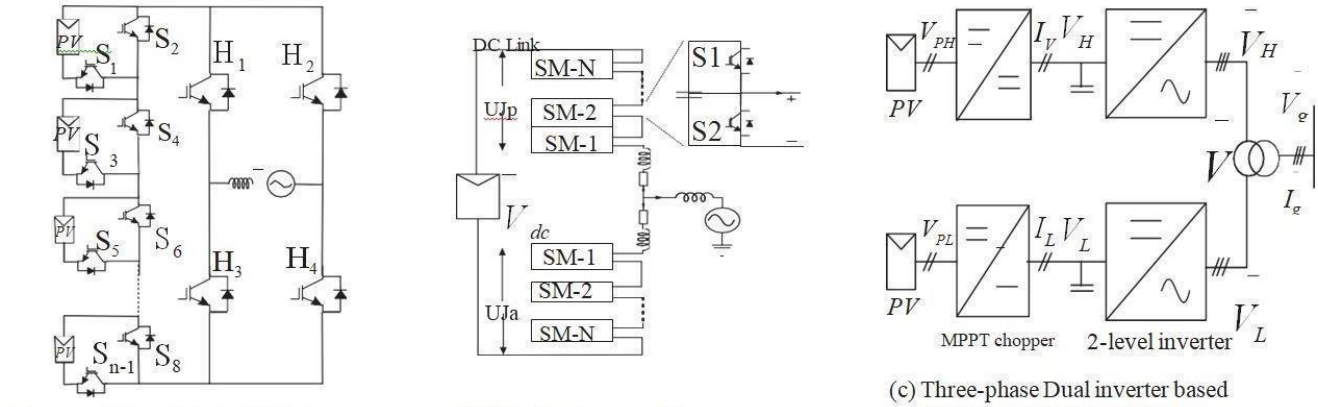
(c) Cascaded T-type inverter (Jana et al. , 2016)

Figure 4: Power circuit of cascaded GCMLIs.

Modular Grid Connected MLI (GCMLI)

Fig. 5(a) shows the generalized power circuit diagram of the Modular GCMLI (Bailu et al., 2015) with cascaded half bridge cells. The circuit comprises cascaded modularized half bridge cells (each half bridge containing two power switches and one DC source) and a full bridge inverter (operating at fundamental switching frequency).As the circuit makes use of half bridge cells connected in series, the number of switches and voltage levels (m) that can be obtained at the inverter output is comparatively higher than the traditional cascaded H-bridge MLI. The single phase Modular GCMLI (Mei et al., 2013) is depicted in Fig. 5(b) comprising of N number of sub modules (SM), an inductor and an equivalent resistor in both the upper and lower arms of the inverter. Each SM equivalent to half bridge is connected to the PV array as DC input, whiles the connection point of the upper and lower arms constitutes the output terminal of the converter. The inverter configuration is very much suitable for very high voltage applications like HVDC transmission and integrated energy storage systems. For the MLIs with a single DC source, the problems linked with common mode leakage current, can be addressed byan

additional three phase reactor or a proper SVM technique. A dual inverter topology as shown Fig. 5(c) (Grandi et al., 2009), where two conventional three-phase two level inverters connected in parallel that generates a line voltage of five levels for the grid connected system. Here, there are two isolated DC sources (PV sources), whichinherently avoids the common mode circulation currents.



(a) Cascaded Modular half-bridge GCMLI (Bailu et al., 2015)`

(b) Single-phase modular GCMLI (Mei et al., 2013)

(c) Three-phase Dual inverter based MLI (Grandi et al., 2009)

Figure 5: Power circuit of modular GCMLIs

Reduced Switch Grid Connected MLI (GCMLI)

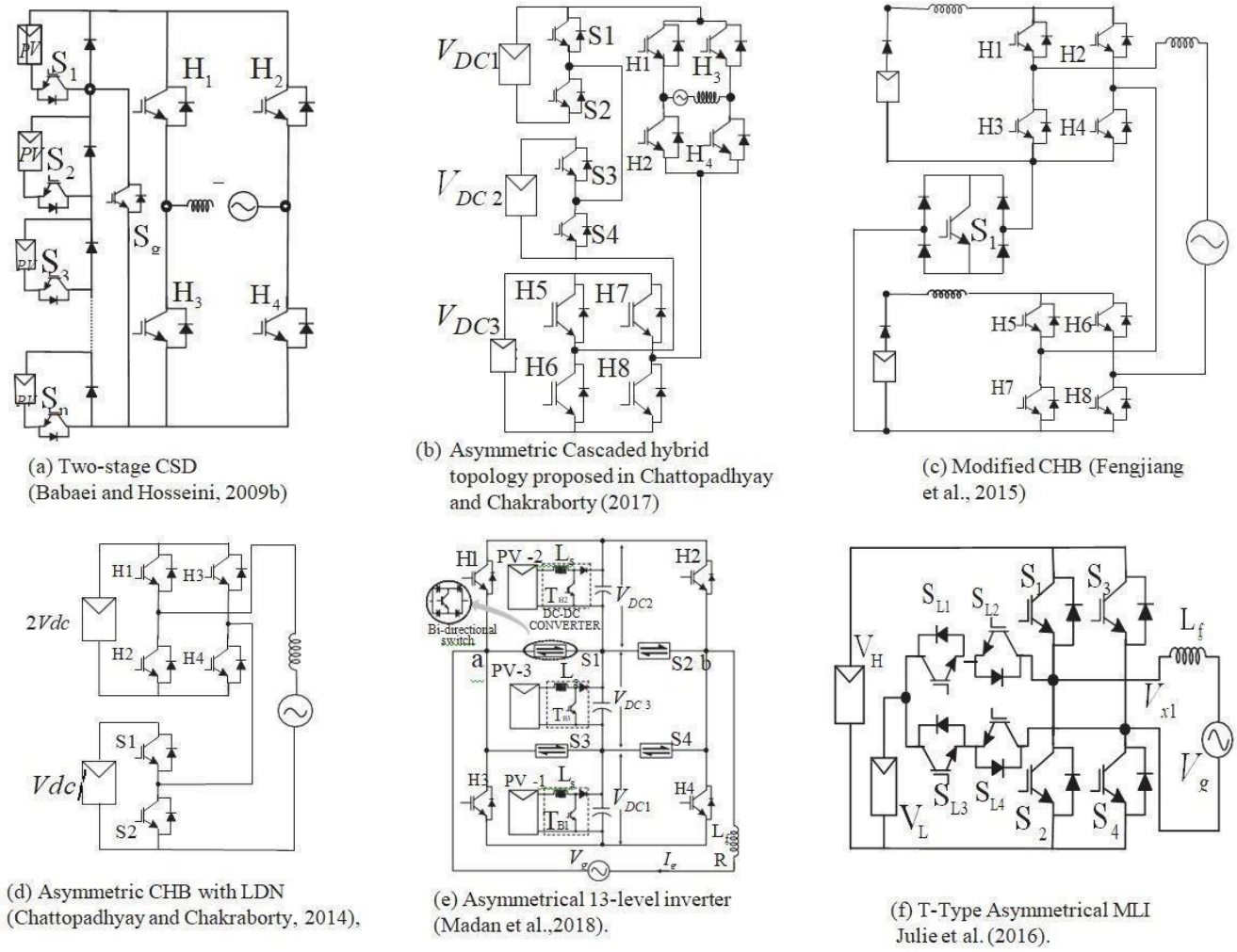
Reduced Switch MLIs are one of the recent topics in the field of power electronics, motor drives and will, as PV arrays can be conveniently used as independent DC sources, be very suitable for sustainable systems in the coming days. Any of the reduced MLI switches have high level components and a H bridge to produce polarity. This definition allows further classification of reduced switch MLIs as defined in the following sub-section.

Reduced Switch Grid Connected MLI (GCMLI) with H-bridge

Here, the topology contains an H-bridge for the polarity reversal, in order to generate an output voltage of m- levels. Fig. 6(a) shows the two stages cascaded switched diode (CSD) MLI topology proposed in Wang et al. The topology is capable of producing more voltage levels with the lesser number of switches as compared to the cascaded half bridge MLI circuit (Babaei and Hosseini, 2009b). As depicted from Fig. 6(a), the circuit is divided into two stages, with first stage having 'n' number of switched diode structure connected in series, while the second stage is a simple H-bridge. In the first stage, the diodes are connected in parallel to the switch so as to avoid the shoot through phenomenon of the bridge arm. Also, a spike removal switch "Sg" is connected from the2nd to nth unit, in order to provide a path for the reverse load current. The circuit can be applied up to the medium voltage renewable energy systems at unity power factor condition only.

A new asymmetric hybrid MLI topology was introduced in Chattopadhyay and Chakraborty (2017), comprising two series connected half bridge cells as the basic unit as shown in Fig. 6(b). This basic unit is then connected in a cascaded manner with one H-bridge cell, in order to attain the proposed configuration. The DC voltage sources in basic unit follow binary sequence, keeping the DC source of H-bridge is constant. One additional H-bridge inverter is required as a polarity generating part which may be connected to the grid also. The Modified Cascaded MLI (MCMLI) was proposed (Fengjiang et al., 2015), to meet the wide range of output voltage and power variation of the PV system as shown in Fig. 6(c). The topology works on the fact that when an auxiliary bidirectional switch (S1) is added into a classic cascaded H-bridge MLI (CHBMLI), the topology can be interchanged between CHBMLI and H-Bridge Inverter (HBI) modes. When the bidirectional switch S1 is off, the circuit operates as conventional CMLI, while it switches to HBI mode with S1 on. The advantages of MCMLI, when working on a large scale are to increase the utilization of PV arrays, reduced harmonic injection and improved power supply quality to the grid.

The Asymmetric full bridge GCMLI with level doubling network (LDN) (Chattopadhyay and Chakraborty, 2014), is depicted in Fig. 6(d). Asymmetrical full-bridge converters with LDN are a combination of full bridge and a half-bridge circuit per phase. The LDN circuit is a half-bridge converter that nearly doubled the voltage obtained by an inverter (here H-bridge). The DC link voltages for the asymmetrical configuration are chosen as 1:2 for a seven level inverter. The LDN circuit is obtained by adding an extra half bridge to the remaining MLI. Two legs comprising one full-bridge converter and one LDN each, with four voltage sources of voltage ratio 14:7:2:1 act as a configuration for the three phase version of the converter. The inverter is found immensely useful for solar PV applications, with an excellent harmonic profile. Also, the converter can extract power from solar arrays under a wide range of varying irradiance and temperature.



(a) Two-stage CSD (Babaei and Hosseini, 2009b)

(b) Asymmetric Cascaded hybrid topology proposed in Chattopadhyay and Chakraborty (2017)

(c) Modified CHB (Fengjiang et al., 2015)

(d) Asymmetric CHB with LDN (Chattopadhyay and Chakraborty, 2014),

(e) Asymmetrical 13-level inverter (Madan et al.,2018).

(f) T-Type Asymmetrical MLI Julie et al. (2016).

Figure 6: Power circuits of reduced switch GCMLIs with H-bridge.

A thirteen level asymmetrical inverter with a smaller number of switches is shown in Fig. 6(e) for a grid-tied photovoltaic system (Madan et al.). The magnitude of DC link voltages (VDC1:VDC2:VDC3) are in the ratio of 1:2:3 to obtain an asymmetrical thirteen level inverter. The proposed asymmetrical thirteen level inverter consists of four unidirectional and four bidirectional switches. The switches H1, H4 and switches H2, H3 will

conduct during the positive and negative half cycles of fundamental output voltages respectively. The switches (S1–S4) as shown in Fig. 6(e), will generate ± VDC1, ± VDC2, ± VDC3 and zero voltage levels. Fig. 6(f) shows the T-Type and NPC-Type dual port Asymmetrical MLIs (DPAMI) respectively, as proposed in Julie et al. (2016). Here, one dc port is connected to a high voltage source VH, whereas the other one is connected to a low- voltage source VL. The new power flow path between the low-voltage source VL and the ac output is built by the proposed DPAMI, thereby supplying partial input power directly from the low-voltage source tothe inverter.

Reduced Switch Grid Connected MLI (GCMLI) without H-bridge

The reduced switch grid connected (GCMLI) without H-bridge has an advantage of fewer numbers of switches. The neutral point clamped (NPC) with multiple PV sources and Capacitive Divider topology, as depicted in Fig. 7(a), is an extension to NPCMLI by adding a voltage source like PV with capacitive divider to which the neutral of the grid terminal is connected (González et al., 2008). The configuration assures the non-injection of the DC current to the grid, reduced current ripple and controlled DC link capacitor voltages. The neutral of the grid terminal (MP1) is connected to the midpoint of the second capacitive divider (MP2), to eliminate the DC current injected to the grid.

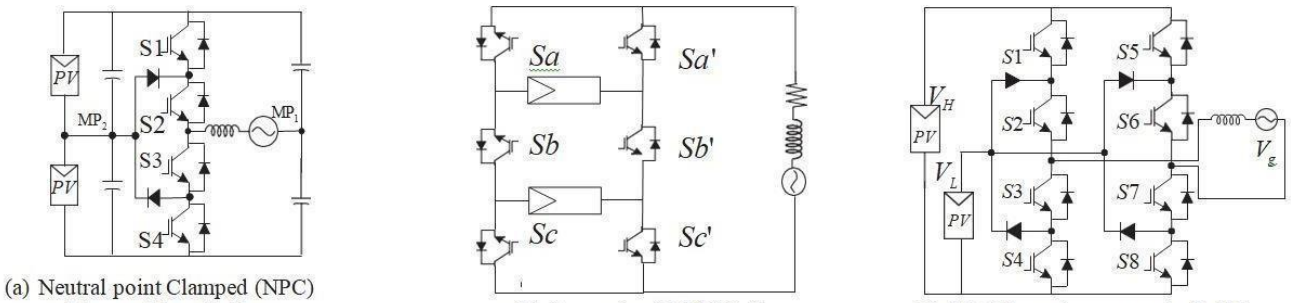
Fig. 7(b) illustrates a seven level Packed U-Cell (PUC) MLI (Julie et al., 2016), which is basically a combinationof FC and CHB inverters. Each U-cell contains two switches and one capacitor. The seven level inverter comprises six switches (Sa, Sb, Sc with their complementary switches Sa', Sb' and Sc') and two isolated DC sources. The upper switches (Sa, Sa') that has to withstand higher voltage must operate at a fundamental switching frequency, while the other four switches (Sb, Sb', Sc and Sc') withstanding small voltages may operateat a higher switching frequency, thereby reducing the switching losses of the inverter. The topology has numerous advantages over other existing topologies as reduced number of power electronics devices, better harmonic profile of output voltage, lower installation cost, etc. Fig. 7(c) shows the NPC-Type dual port (DP) Asymmetrical MLI, as proposed in Wu et al. (2017). Here, one dc port is connected to a high- voltage source VH, whereas the other one is connected to a low-voltage source VL. The new power flow path between the low voltage source VL and the ac output is built by the proposed DP asymmetrical MLI, thereby supplying partial input power directly from the low voltage source to the inverter.

Hybrid Grid Connected MLI (GCMLI) Topology

Hybrid MLI is a result of a combination of any two traditional MLI topologies, a reduced switch and a traditional MLI or two reduced switch MLIs (Silva et al., 2010; Veenstra and Rufer, 2005). The purpose of Hybrid MLI is to improve the harmonic profile and quality of output voltage waveform. Fig. 8(a) depicts a hybrid ANPC converter with cascaded H-bridge cells (Zhou et al., 2009). The purpose of introducing CHB cells is to increase the number of levels without any variation in overall power. The CHB cells act as active power filters to enhance the output power quality. A hybrid nine level GCMLI with minimum number of switches is shown in Fig. 8(b), which basically combines the properties of NPC, FC and coupled inductor based multilevel inverter (Roy et al., 2016). Two DC link capacitors (C1, C2) are used to split a DC source into two, while the third capacitor is maintained at a voltage equal to one fourth of the DC link voltage. Both the ends of coupled inductor are designated properly so as to obtain the desired output voltage waveform of ninelevels.

Fig. 8(c) shows the hybrid T-type NPC (TNPC) and Flying Capacitor H-bridge (FC H-bridge) topology of the 9- level inverter proposed in Sandeep et al. (2017). The circuit is modular

in nature and used a lesser number of switches, diodes and capacitors. The dc-link capacitors and FC voltages are maintained at Vdc/2and Vdc/4, respectively. Hence, the inverter is capable of generating nine levels of output voltage: ± Vdc, ± 3Vdc/4, ± Vdc/2, ± Vdc/4 and 0. The configuration can also be extended by adding FC H-bridges, to generate a higher voltage level. Also, an advantage of this inverter is that the circuit will always operate as a five-level inverter even if FC H-bridge fails.



(a) Neutral point Clamped (NPC) with capacitive divider (González et al., 2008)

(b) Seven-level PUC (Julie et al., 2016)

(c) NPC Type Asymmetrical MLI (Wu et al. , 2017)

Figure 7: Power circuits of reduced switch GCMLIs without H-bridge.

Fig. 8(d) depicts the schematic circuit diagram of five-level hybrid MLI, comprising two half-bridge (S1 and S2, S3 and S4) and one full bridge structure (H1–H4) (Sandeep et al., 2018). The switches S3 and S4 are bidirectional, while the remaining ones are unidirectional switches. The switches S1 and S2 are complementary in nature and are used to generate voltage levels Vdc and Vdc/2. The switches (H1–H4) generate the positive, negative, and zero levels of voltage across the load. The bidirectional switches S3 and S4 provide the freewheeling path during zero voltage state. The topology can be extended in cascaded fashion and is capable of minimizing leakage current in a photo voltaic system.

Modulation Techniques Used for GCMLI

As the multi-level inverters used a large number of switches to generate the stair case output voltage, the sequence in which switches operate and the duration of each step are very vital in minimizing the total harmonic distortion (THD). The pulse width modulation (PWM) techniques for GCMLI can be broadly classified as Fundamental switching frequency, high switching frequency and variable switching frequency. The fundamental switching frequency modulation technique is that one where a switch has one or two

commutations per cycle; whereas, the high switching frequency modulation has multiple commutations per cycle (Zhao et al., 2010b). Fig. 9 represents the detailed classification of different modulation techniques for a GCMLI, which are explainedin the upcoming section.

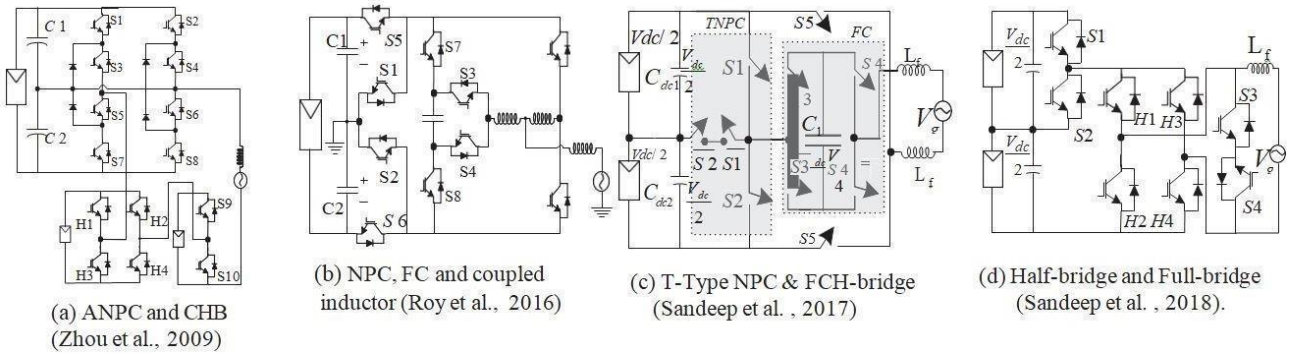


Figure 8: Power circuits of different hybrid GCMLI topologies.

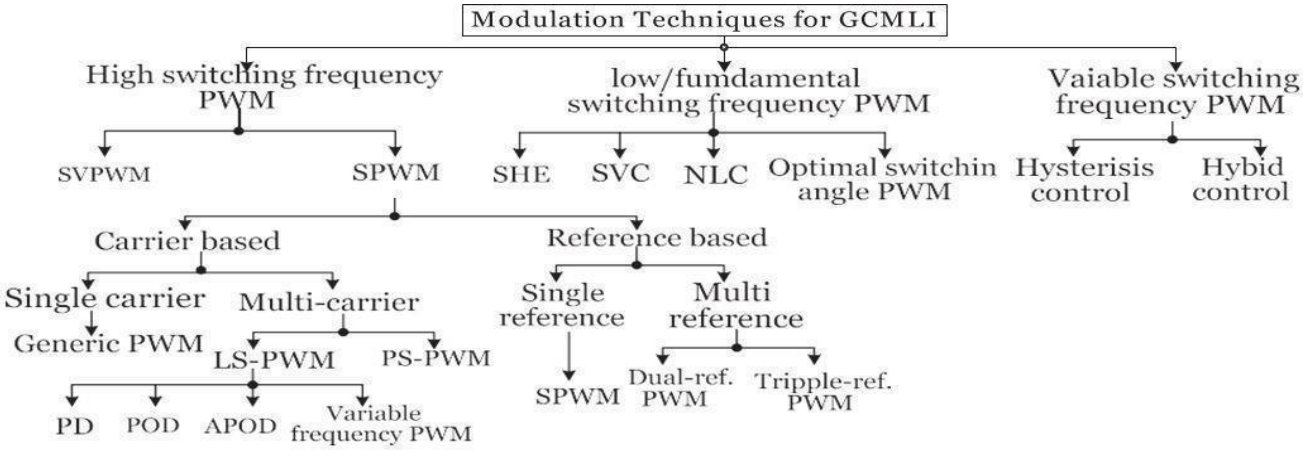


Figure 9: Classification of the modulation techniques used in different GCMLI topologies.

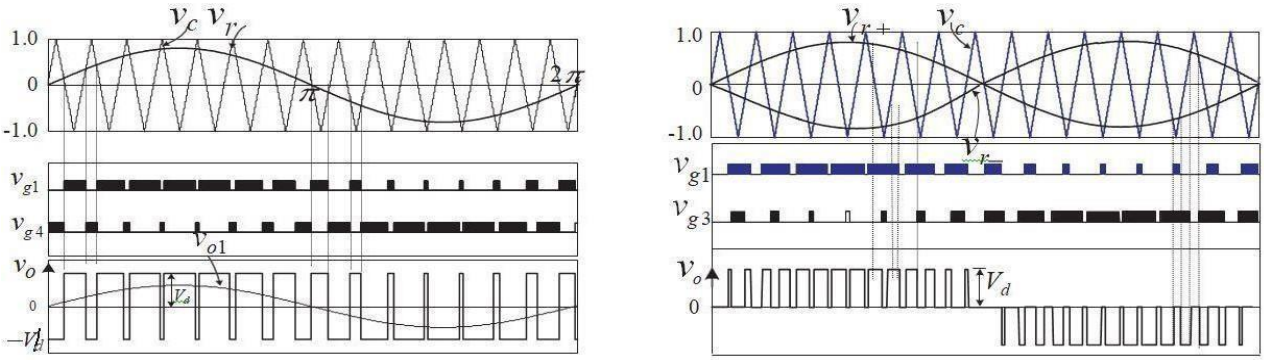
High Frequency Modulation Techniques

The high frequency modulation techniques for the MLIs to generate the gating signals are not unique. Several methods that are proposed in the literatures make use of such technique, which is classified and described in the following section.

Sinusoidal Pulse Width Modulation (SPWM)

Sinusoidal Pulse Width Modulation (SPWM) is one of the popular modulation techniques for any inverter. The SPWM technique is for a conventional two level inverter comprising bipolar and unipolar PWM techniques, as shown in Fig. 10. In bipolar PWM technique, one reference signal (Vr) is compared with the carrier signal (Vc)to generate the gating signal (in Fig. 10(a)) for the inverter, whereas, for the unipolar technique, two reference signals of opposite phases are compared with the same carrier signal to generate the three level voltage as shown in Fig. 10(b). This SPWM technique is widely used in conventional as well

as multi-level inverter based grid connected system (Carrara et al., 1992). As the major concern with high power GCMLI is Power dissipation, the multi-carrier SPWM control methods (Carrara et al., 1992; Naderi and Rahmati, 2008; Mcgrath and Holmes, 2002; Zhao et al., 2010a; Alexander, 2016; Kumar and Narayanan, 2016; Vadhiraj et al., 2013; Sahoo and Bhattacharya, 2018; Roberto et al., 2011) are preferred as they enhance the efficiency of multilevel inverters in high power applications. For any multilevel inverter, the above SPWM technique can be extended using multiplecarriers. The multi-carrier based SPWM techniques are classified based on the number of carriers, references andtheir disposition discussed in the following section.



(a) Unipolar SPWM (b) Bipolar SPWM

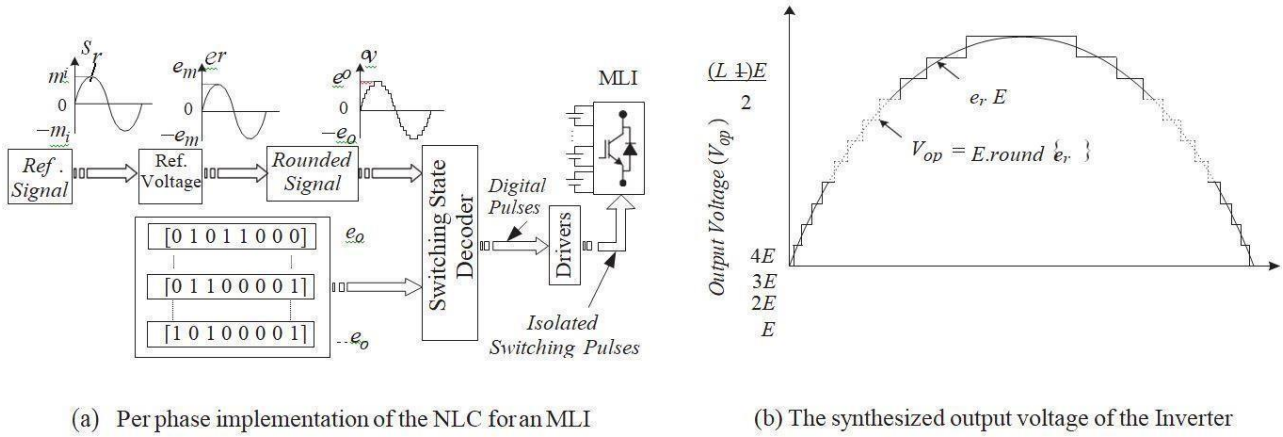
Figure 10: SPWM techniques (Carrara et al., 1992).

Low Frequency Modulation Technique

Several low frequency modulation techniques like Nearest Vector Control (NVC), Nearest Level Control (NLC) and Nearest Level Modulation (NLM) techniques are also used for some high power applications. The main objective of the NVC control, also known as space vector control, is to find out the closest vector to the referencevector which minimizes the space error between them (Choudhury et al., 2016; Deng and Harley, 2015). The NVC control technique is best suited for MLIs with higher number of output voltage levels as the higher density of vectors reduces the probability of generating error signals which will further lead to reduced THD and ripplein the output waveforms. However, the lower order harmonics as the technique requires low switching frequency; lower order harmonics can't be eliminated by this method.

The Nearest Level Control (NLC) is used to compare the sinusoidal reference with the output voltage of inverter in order to select the nearest voltage level. The different stages of NLC that synthesizes the output voltage waveform are depicted in Fig. 11(a) and (b) respectively. As it is easier to locate the nearest voltage level than the NVC method and also, the technique offers better quality of output voltage and a smaller ripple in load current (Mei et al., 2013; Converter et al., 2015), the NLC technique is very suitable for high level inverters. The nearest level modulation (NLM) method has a unique advantage of controlling the phase voltages of the converter directly. Here, the reference voltage is approximated using any pair of voltage levels (Edpuganti and Rathore, 2015). Then the

approximation is extended to all the existing pair of voltage levels and the mean of all the reference levels is calculated, which is then the actual value of the reference voltage. The higher the frequency, the better is an approximation of the reference signal.



(a) Per phase implementation of the NLC for an MLI (b) The synthesized output voltage of the Inverter

Figure 11: Different stages and synthesized output for NLC (Converter et al., 2015).

Characteristics of NLM and NLC Techniques

The NLM and NLC techniques use less computational time and complexity compared to the PWM techniques like SVPWM and SHE. NLM gives an excellent dynamic performance, which is required for the grid synchronization and for the efficient MPPT. The NLC technique directly computes switching states and duty cycle for each phase of the MLI, thereby avoiding the necessity of triangular carrier signal.

Optimal Switching Angle PWM

The harmonics in the inverter voltage waveform can be minimized by calculating the optimal value of switching angle. The arrangement of switching angle is very important so as to improve the power quality of the output waveform. It is very important to calculate switching angle without any error, so as to obtain the output voltage waveform perfectly (Jinghua and Zhengxi, 2013).

Switching Angle Calculation Techniques

The switching angle (γ) is defined as the instant at which the voltage level of the inverter changes. Fig. 11 represents the generalized MLI output voltage waveform which is symmetrical in nature. Generally, the m-level inverter requires (m − 1)/2 number of main switching angles. The switching angles corresponding to the second, third and fourth quadrant can be calculated as (π − γ 1). (π + γ (m−1)/2) and (2π − γ 1) respectively given in Babaei and Gowgani (2014). The comparative analysis of four techniques for the switching angle calculation methods have been discussed in the Table 2.

Table 2: Comparative analysis of different switching angle calculation methods

Switching angle (γ) calculation methods	Switching angle γ, for i = 1, 2 ... (m − 1)/2	Nature of γ	THD in output voltage	Remarks
Equal-phase	$\gamma_i = i\,(180°/m)$	Very narrow	High	Preferred for inverters with smaller output voltage levels.
Half-equal phase	$\gamma_i = i\,(180°/m + 1)$	Narrow	High	Preferred for inverters with smaller output voltage levels.
Half-height	$\sin^{-1}\left(\frac{2i-1}{m-1}\right)$	Wide	Medium	Preferred for small and medium voltage levels.
Feed-forward	$\sin^{-1}\left(\frac{i-0.5}{m}\right)$	Very wide	Small	Most preferable technique for any level of output.

General Modulation Strategies of Hybrid Modulation Strategy

Although, the high frequency modulation methods (SPWM, SVPWM, etc.) offer low current harmonic distortionand produce high frequency output voltage waveform, yet they lead to high switching losses which are not desirable for high voltage applications. Hybrid-modulation strategies (Govindaraju, 2011b; Alexander, 2016; Karampuri et al., 2017; Moeini et al., 2017b) represent combinations of fundamental-frequency modulation and multilevel sinusoidal-PWM (MSPWM) strategies. A hybrid PWM scheme has been presented in Karampuri et al. (2017), comprising SVM and SHEPWM. The SHEPWM and SVM are performed to achieve better steady state and dynamic performance in faulty grid conditions respectively. The paper Karampuri et al. (2017) also proposed a suitable strategy that enables fast and smooth transition between SVM and SHE modulation schemes. Another Hybrid modulation technique proposed in Moeini et al. (2017b) consists of selective harmonic current mitigation (SHCM- PWM) under steady state and phase-shift PWM (PSPWM) under transient conditions. This technique was preferred to extend the modulation range of inverter and process active and reactive power operation in all the four quadrants. Fig. 11 depicts the block diagram of modulation technique proposed in Moeini et al. (2017b). Here, the modulation selector block functions as per change in the current references (I∗) in-d and q axes. If the current references in both the axes are greater than zero, PSPWM is used, else SHCM PWM is opted.

Hysteresis PWM

In Hysteresis PWM, the current error signal and fixed width hysteresis band are compared, in order to generate the switching signals for inverter (Suhara and Nandakumar, 2015). The modulation technique suffers from the drawback that the performance of of active power filter gets affected as soon as the phase current is injected. However, these drawbacks can be overcome by the methods discussed (Chen and Xie, April 2004).

Characteristics of Hysteresis PWM

The hysteresis modulation technique has extreme robustness, greater stability and faster dynamic response ascompared to other PWM techniques.

Control Techniques of a Grid Connected Multilevel Inverter (GCMLI)

The grid connected multilevel inverters (GCMLIs), require a suitable control technique in order to inject pure sinusoidal current to the grid, which should also be in the same phase with grid voltage so as to maintain the unity power factor (Jana et al., 2016) and minimize the reactive power. Thus, the whole active power should be transferred from PV panels to the grid, maintaining the overall DC link voltage higher than that of the peak voltage of the grid (Madan et al.). For the MLI with multiple DC sources, the controller should independently regulate the DC link voltages; so that the maximum power can be extracted from each of the PV panels (Grandi et al., 2009). The controller should also be able to maintain the system stability during varying weather conditions like variable irradiation and temperature (Madan et al.). It should also provide selective compensationin order to minimise load current disturbances, by means of harmonic or reactive current compensation (Silva, 1997). For a hysteresis current controller based GCMLI, it should try to maintain a constant switching
frequency for safety purposes and low switching losses (Mostafa et al., 2013). Fig. 11 depicts the classificationof control techniques that are applicable to a single phase/three phase GCMLIs. The different control theories mentioned in Fig. 11 are applicable in the control strategies discussed in the upcoming section.

Control Techniques for Single Voltage Sourced GCMLS

Several control techniques have been reported for the grid connected applications (Tsengenes et al., 2012; Busquets-Monge et al., 2008), using the single source MLI as depicted in Fig. 3. For the control of neutral point clamped (NPC) GCMLI, five distinct techniques are discussed here, namely, the voltage oriented control (VOC) (Schaefer et al., 2017); direct current control (DCC) (Utkin, 1993), sliding mode control (SMC) (Sebaaly et al., 2016) and outer voltage and inner current closed loop control (Busquets-Monge et al., 2008).

The VOC control technique (Tsengenes et al., 2012) is commonly used in the control of PQ compensators and interfaced inverters in distributed generation (DG) systems. It illustrates a modified version of VOC method where the PV system operates as a shunt active power filter (APF), a reactive power compensator and a load current balancer simultaneously. In this way, the PV system operates more efficiently compared to the traditionalPV systems and offers supplementary services to the utility grid. The controller relies on the space vector modulation (SVM) technique. The above control method is limited to a three-level inverter only, whereas the DCC technique (Utkin, 1993) is applicable to m-level inverters. This control technique not only controls the line current (iabc) very accurately, but also delivers a robust and dynamic behavior even under system fault conditions. The controller as depicted in the includes the measurements and filtering of the grid current (i*abc) as well as the three-phase (a-b-c) to the two-phase orthogonal α–β and non-orthogonal a*b* coordinate transformation blocks, that determine the space vectors easily for a space vector based control system. To filter the grid current measured, a sinc3 filter along with the multiple second order

generalized
integrators (multi- SOGI) are used. The output of the current controller is passed through the dc-link balancing algorithm which determines the switching vector whose purpose is to minimize the deviation of the capacitor voltage. The sliding mode control (SMC) is one of the most popular non-linear control technique for a GCMLI, as it is robust, has good dynamic response and highly compatible with the switching pattern of inverter (Sebaaly et al., 2016). However, SMC suffers from the chattering problem that leads to a variable and high switching frequency triggering pulses, resulting in higher switching losses. A fixed frequency PWM based SMC is proposed in Busquets-Monge et al. (2008) as shown in Fig. 18(c) that compensates the chattering problem by adopting Gao's reaching law. The adoption of this control technique requires only L-filter that results in an accurate tracking response, low THD and ripple for the grid injected current as well as it stabilizes the DC bus voltage under external perturbations. Fig. 18(d) shows a flexible and highly efficient current controller for an NPC inverter that can work well in steady state and transient conditions (Wang et al., 2013). The controller not only has the ability to track the reactive power variations at a higher speed, but also compensates the current components at all switching frequencies. A unique feature of this controller is that it can be extended to any such converter topologies and can be used in distributed power generation systems also.

The control technique of a flying capacitor multi-cell (FCM) converter based active power filter (AFC) for a gridconnected PV system (Pouresmaeil et al., 2012) is shown in Fig. 18(e). The reference current (Iref) of the predictive current controller for the APF is determined by the instantaneous values of P and Q using P-Q theory.According to this inverter, the modular multi-level converter (MMC) as discussed in Mei et al. (2013), when used in conjunction with the PV-grid system, arises serious issues. The circulating current of the MMC not only intend to affect the system stability, but also reduces the overall inverter efficiency. The work done in Mei et al. (2013) considers the problems imposed by the uncontrolled circulating current of MMC. Here, a new PWM method called selective virtual loop mapping (SVLM) is proposed. The mapping routines among Virtual sub- module (VSM) and the real sub-module (RSM) are changed in order to balance the capacitor voltages in both ofthe arms of the bridge. The controller has a unique advantage that it can be realized for large scalegeneration.

Control Techniques of Multiple Voltage Source Fed Symmetric GCMLI

Several multi-level inverters with multiple DC link voltage sources like PV sources have been discussed in Section 3.2. In a CHB based GCMLI, as the entire H-bridges share the same amount of grid current, it is a necessity to implement a unique grid current control loop. A controller has been proposed in Villanueva et al. (2009), for a single-phase CHB converter with 'n' number of modules. The controller includes 'n' numbers of outer voltage loops to maintain their DC link voltages (Vdc) constant and one inner current loop for the generation of a sinusoidal reference current (ig*) with unity power factor. However, nothing is

mentioned about the power mismatch and stability of the system with variations in solar irradiance and temperature. The control of a three phase dual inverter topology presented in Grandi et al. (2009) comprises a dc voltage controller to adjust the dc link voltages of two three phase, two level inverter bridges (VH and VL) P-Q theory, the three phase voltages (vL) and currents (iL) are trans equal to a common reference voltage, V* formed into the two- phase α-β components and P-Q components are determined. On the other hand, the reference voltage (Vref) for the APF can be determined using the predictive current control technique. When active neutral point clamped (ANPC) converters are used with grid connected photovoltaic system, the capacitors can experience a pulsed power and arises a dc-link unbalancing issue. The selection of the reference voltage value for the flying capacitor(FC) can play an important role to balance the average values of the dc-link capacitor voltage. Two control schemes for the grid connected system, where the performance of the conventional modulator (Wang et al., 2013) is compared with the proposed modulator (Teymour et al., 2015). In the conventional, the controller can only produce and change the desired output voltage (v*) of the converter, and the FC voltage is always regulated to Vdc/4. Whereas, the proposed control strategy used an additional reference voltage (v*fc) for the FC as an input of the modulator, which adds an additional freedom to control the system. These new features balanced the dc-link capacitor voltages as well and achieve a better quality voltage. In a GCMLI system, where the series connected PV arrays feed the inverter, the mismatch of power between the PV arrays leads to the reduction of PV output.

This power mismatch problem in the PV arrays is very efficiently addressed in the controller proposed in Busquets-Monge et al. (2008). A DC link controller block is used to balance the total DC link voltage, an unbalanced control block handles the partial shading problems of the individual PV arrays and a modulator blockgenerates the inverter switching pulses. The modulator block generates the gate pulses of the three phase four level NPC with a variable duty ratio by using the virtual vector based PWM. This control scheme not only regulate the PV array voltage independently to its MPP, but also improves the quality of output voltage, allows atransformer less operation and increases the efficiency of the two PI called as sigma (Σ) and delta (Δ) controller. The sigma controller generates the reference current for the grid in such a way that both the inverter generates the same current injected to the grid through the open end winding transformer. For this, a current controller based on the feed forward action of the voltage is adopted. A modified space vector modulation (SVM) technique is used to generate the gate pulses for the MLI. The controller not only deals with variations in temperature and irradiance conditions, but also performs well under any operating conditions. However, the control strategy cannot be extended for an MLI having more than two inverter bridges. A conventional control scheme for energy balance controller of the CHBMLI has been proposed (Chavarría et al., 2013), based on an energy sampled data model of the PV system. For the closed loop dynamics of energy balance controller for kth Inverter Bridge, as shown in Fig. 19(c)-i, a digital PI controller has been chosen. The design guide lines mentioned in Dell et al. (2008) and Chavarría et al. (2006), confirms the fast dynamic response, zero steady stateerror at the tracking frequency, and achieve a local stability of the controller. In addition to this, by designing a current controller, the inverter output

current (iL) tracked the reference current (i*) set by the energy balance controller as shown in Fig. 19(c)-ii. Also, a proper control system is used for the CHB converters as the active power mismatch in modules of CHB inverter may lead to unsymmetrical ac output voltage, over-modulation and degraded power quality. However, the control strategies proposed in Chavarría et al. (2013), Dell et al. (2008), Chavarría et al. (2006), and Zmood and Holmes (2003) did not consider the leakage current issues, due to which the PV arrays cannot be directly connected to the individual converter module in high voltage large scale PV system applications. These aforementioned issues were solved by using a decoupled active and reactive power controller (Liu et al., 2015) for a large scale grid connected cascaded PV system including the current fed dual active bridge (CF-DAB) dc–dc converters and cascaded multilevel inverters. It controls the duty ratio (D) as well as the phase shift angle (ϕ) through PI and PR controller to control the respective PV voltage (Vpv1a_1) and lowvoltage side (LVS) dc link voltage. The bandwidth of the PI controller is chosen considerably high to block the double frequency component from the PV whereas, the gain of PR controller is considered high to follow the LVS voltage exactly equal to the reference voltage. On the other hand, the controller of the CHBMLI consists ofthe individual outer voltage loop for controlling the dc voltage of each inverter module to track the reference Vdc generated by the PI controller.

Comparative Analysis of Different Controllers for GCMLIs

The different grid management techniques suggested for different MLIs (GCMLIs) is analyzed in the literature. The comparison is based on the various strategies suggested for the grid current tracking, the DC bus voltage regulation techniques, the d-q axis current and the voltage components for the three-phase system, and the modulation techniques implemented for their application on a system connected to the grid. In addition, for the better assessment of device performance, the essential features suggested by the controllers are included for different GCMLIs.

Conclusion

Due to their better voltage qualities than traditional two level inverters, MLIs are increasingly used on grid interfaces with renewable energy sources. This paper classifies and explains detailed MLIs for grid-connected systems based on the number of voltage sources. For grid-connected applications some reduced switch MLIs are also presented. If asymmetric voltage sources are used for MLI, the voltage efficiency is considerably improved and the number of components minimized. The MLI also fulfills very effectively the strict grid codes for the gridinterfacing. The PWM technic for the GCMLIs is detailed classified on the basis of the switching frequencies as the PWM technics determine the frequency of switching and thus the rips and harmonics in the inverter stress. The monitoring strategies for different GCMLIs are categorized according to the controls and MLI types. It was found that the GCMLI control plays a crucial role in completing the grid codes and optimizing power pumped into the grid by a unitary power factor with the sinusoidal current. A detailed comparative analysis is proposed between the different MLI topologies, their modulation and regulation of different applications linked to one and three phases of the grid. It is observed to increase the efficiency of network linked energy

sources even at lower frequencies with less filter components by means of the MLIs with adequate power. A selection of a suitable MLI and its control technique can also resolve a number of GCMLI issues, such as DC connecting voltage balances, power blends, systems reliability under variable inlets and grid components.

CONFLICTS OF INTEREST

There are no financial issues or interest of conflicts to declare.

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